

(3 Hours)

Total Marks: 80

- 1) Question No. 1 is compulsory.
- 2) Solve any three from remaining five questions.

- a) Compare FPGA and CPLD
  - b) Draw carry circuit for 3-bit CLA adder using MOS
  - c) Draw layout for inverter using lambda rules
  - d) Draw D flip flop and write HDL program for it
  - e) Explain clock distribution scheme
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- a) Implement full adder circuit using CMOS
  - b) Design circuit for 4-bit Carry skip adder
  - c) Implement  $Y = \overline{AB} \cdot (C + DE)$  using following design styles:
    - 1) Static CMOS 2) Dynamic CMOS 3) Clocked MOS(C2MOS) 4) Pseudo NMOS
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- a) Draw 4-BIT ripple carry adder using Full adder and Write program for it using HDL 10
  - b) Design Sum of absolute differences using RTL design technique. Draw HLSM, Datapath, Interface and Controller FSM 10
  - a) Explain SRAM and its operation with proper diagram 10
  - b) Draw 4x4 bit NOR based ROM array to store the following data in respective memory locations 10

Memory Address	Data
1000	0111
0100	0101
0010	0110
0001	1001

- a) Design RTL for Serial FIR filter. Draw HLSM, Datapath and FSM 10
- b) Implement clocked S-R latch using CMOS and draw layout for it using Lambda design rules 10
- Write short notes:
  - a) ESD Protection 05
  - b) Clock Generation 05
  - c) Interconnect delay model 05
  - d) Flash Memory 05

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