

QP : Code : 25071

[Total Marks : 80

(3 Hours)

Question no. 1 is compulsory.

) Solve any three questions out of remaining.

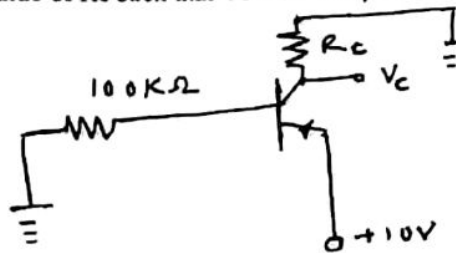
) Fig. to the right indicates maximum marks.

) Assume suitable data wherever necessary but justify the same.

any five.

(5x4 = 20)

Determine the value of R_c such that $V_c = 5V$ and $\beta = 50$.



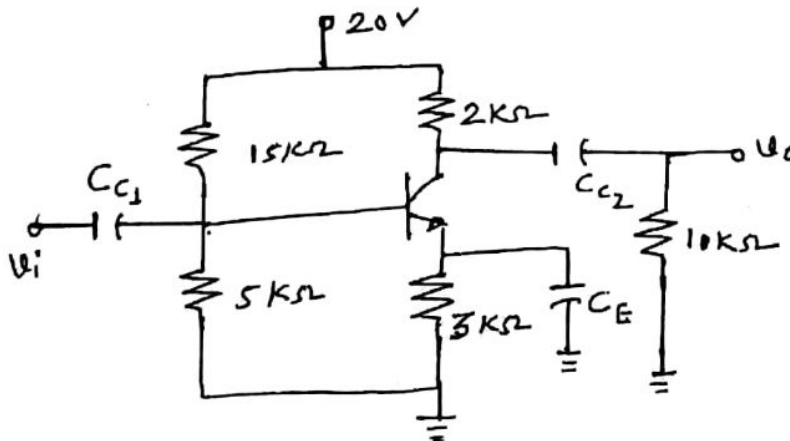
State and explain Miller's Theorem.

Design a self bias circuit using JFET for $I_D = 3mA$, $V_{DD} = 20V$ and $V_{DS} = 0.6 V_{DD}$.

($I_{DSS} = 8mA$, $V_p = -4V$)

Explain various types of capacitors.

Determine the values of coupling capacitors C_{C1} and C_{C2} if $r_{\pi} = 1.5K\Omega$, $\beta = 120$ and $f_L = 20Hz$.

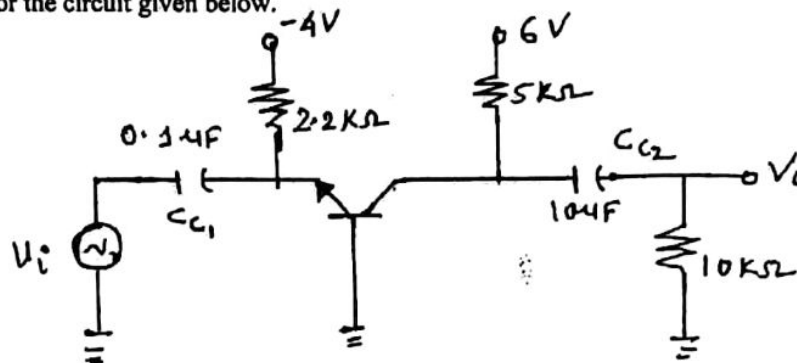


Explain concept of zero temperature drift in JFET.

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Q2. A) Calculate 1) I_{BQ} , I_{CQ} 2) g_m , r_{π} 3) Small signal voltage gain 10

For the circuit given below.



Q2 B) Explain the concept of LC filter in power supply circuit and hence derive expression for ripple factor of LC filter. 10

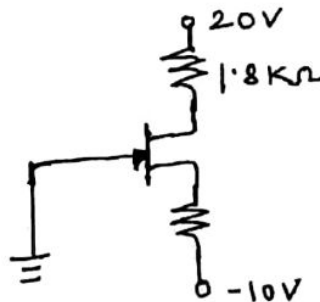
Q3 A) Explain concept of shunt Zener regulator. For a shunt Zener regulator giving 10

output voltage of 10 V and load resistance varying from $5K\Omega$ to $10K\Omega$, V_{in} is varying between 18V to 22V.

Find R_s , P_{zmax} , S_v and R_o .

Assume $R_z = 4\Omega$ and $I_{zmin} = 50\mu A$.

B) Determine I_{DQ} , V_{GSQ} , V_{DSQ} if $I_{DSS} = 9mA$ and $V_p = -3V$ for the circuit given below. 10



Q4 A) Design capacitive filter with FWR using two diodes with ripple factor less than 5%. 10

Output voltage is 24V and load current 200mA. The input line voltage of 230V/ 50Hz is available.

B) Determine the values of biasing components for a CE configuration if $V_{CC} = 12V$, 1

$V_{CE} = 6V$, $R_C = 1K\Omega$, $V_{BE} = 0.6V$, $\beta = 180$ for the following circuit.

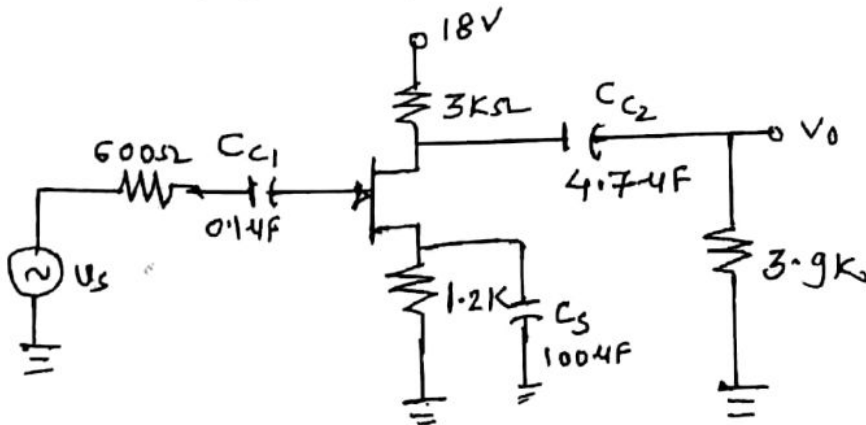
i) Fixed bias without R_E

ii) Voltage Divider bias with $V_{RE} = 10\%$ of V_{CC} and $S_1 = 8$

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For JFET if $I_{DSS} = 6 \text{ mA}$, $V_p = -6 \text{ V}$, $r_d = \infty$, $C_{gd} = 4 \text{ pF}$, $C_{gs} = 6 \text{ pF}$, $C_{ds} = 1 \text{ pF}$ 15

- Determine i) V_{GSQ} ii) I_{DQ}
 iii) g_{m0} iv) g_m
 v) Midband voltage gain A_v
 vi) Higher cut off frequency



B) Explain high frequency \square equivalent model of common emitter BJT. 5

16. Design single stage CS amplifier using mid-point biasing method for voltage gain of 12, 20

$F_L = 20 \text{ Hz}$, $R_L = 10 \text{ K}\Omega$, $V_o = 3.5 \text{ V}$

(Use JFET parameters $I_{DSS} = 7 \text{ mA}$, $V_p = -2.5 \text{ V}$, $g_{m0} = 5600 \mu\text{S}$, $r_d = 50 \text{ K}\Omega$)

Recd " 27

3.5) PM on 28.11.18


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2 (a) Take $\beta = 110$

3(b) Take $R_S = 1.5 \text{ k}\Omega$

5 (a) Take Gate resistance $R_g = 1 \text{ M}\Omega$

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28/11/18

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